OPTOELECTRONIC DEVICE USING A DISABLED TUNNEL JUNCTION

FOR CURRENT CONFINEMENT

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BACKGROUND

[0001]   Optoelectronic devices such as vertical cavity surface emitting lasers (VCSELs) covert electrical current into light that can be used in optical communication signals or for other uses. The currents in such devices generally must be confined to specific regions for efficient conversion that minimizes power consumption and maintains a desirable optical field profile. Accordingly, such devices generally have current blocking structures that confine current to the desired regions. These current-blocking structures can be formed using a variety of techniques such as implantation, lateral oxidation, and etching with or without subsequent re-growth. All of these techniques have difficulties and limitations.

[0002]   Implantation for current confinement relies on damaging the crystal lattice of a material in the optoelectronic device to render the material non-conductive. The nature of ion implantation processes causes poor localization of the implanted region. As a result, the boundary between an implanted region and a non-implanted region is soft, which leads to current flow through mildly implanted regions. Additionally, the implant can introduce defects that eventually lead to device degradation.

[0003]   Lateral oxidation for current confinement is currently the method of choice for high performance VCSELs. Lateral oxidation can achieve a very sharp current aperture that for small (<10 μm) devices results in much higher performance than implantation can achieve. However, the oxidation process typically changes a material with a high aluminum concentration into oxide of the same material and is therefore very disruptive to the crystal

lattice. As a result, device degradation that can be traced to the oxidation is seen in VCSELs that use lateral oxidation for confinement.

[0004] Optoelectronic devices with etched features tend to provide poor performance unless a complicated and costly re-growth is performed. Further, for VCSELs, re-growth has so far been unable to provide the high performance found in other semiconductor diode lasers.

[0005] New current confinement techniques are sought to overcome the limitations of the known techniques used in optoelectronic devices.

SUMMARY

[0006] In accordance with an aspect of the invention, a semiconductor optoelectronic device such as a vertical cavity surface emitting laser (VCSEL) includes a tunnel junction that is rendered inoperative in selected areas. The tunnel junction can be produced during epitaxial growth for the semiconductor device and is an operating feature of the semiconductor device. Where operative, the tunnel junction changes the majority carriers for the current in a semiconductor from electrons to holes. Specific areas of the tunnel junction are rendered inoperative to define a current blocking region. Where inoperative, the tunnel junction acts as a standard reverse biased diode and blocks current. A variety of mechanisms including implantation, diffusion, impurity induced disordering, and etching with re-growth can render specific areas of a tunnel junction inoperative.

[0007] One specific embodiment of the invention is an optoelectronic device such as a VCSEL. The optoelectronic device includes: an active region typically composed of layers of (Al)GaAs; a p-type semiconductor region typically a layer of p-type (Al)GaAs; an upper and lower n-type semiconductor region typically layers of n-type (Al)GaAs; a tunnel junction between the p-type and upper n-type semiconductor regions; and a current blocking region between the active region and the n-type semiconductor region. The current blocking region operates as a reversed biased PN junction and confines a current that flows between the active region and the semiconductor region so that the current flows through the tunnel junction.

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[0008]   The current blocking region can have substantially the same structure as the tunnel junction and can be a portion of the tunnel junction in which tunneling has been disabled. For example, the current blocking region can be a portion of the tunnel junction that contains additional dopants that disable tunneling or a portion of the tunnel junction that has a disrupted crystal structure. Alternatively, a feature of the tunnel junction can be etched away or otherwise absent from the area of the current blocking region.

[0009]   Another embodiment of the invention is a method for fabricating an optoelectronic device such as a VCSEL. The fabrication method begins by forming an active region or layer and a semiconductor region or layer with a tunnel junction between the two. Tunneling is then disabled in a selected part of the tunnel junction to form a current blocking region. During operation of the optoelectronic device, the tunnel junction conducts a current of holes tunneling between the active region and the semiconductor region. The current blocking region acts as a reverse-biased PN junction to block current.

[0010]   Tunneling can be disabled using a variety of techniques. Such techniques include but are not limited to: implanting dopants into the selected part of the tunnel junction; diffusing N-type or P-type dopants into the selected part of the tunnel junction, disrupting crystal structure in the selected part of the tunnel junction, and disordering the structure of the tunnel junction with an impurity-induced or an impurity-free disordering process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]   Fig. 1 shows a cross-sectional view of a VCSEL having a contact on the back of the wafer and a tunnel junction in accordance with an embodiment of the invention.

[0012]   Fig. 2 shows a cross-sectional view of a VCSEL grown on a p-type or nonconductive substrate to allow device isolation and having an N-type layer under the active layer and a tunnel junction in accordance with an embodiment of the invention.

[0013]   Fig. 3 shows a cross-sectional view of a VCSEL in accordance with an embodiment of the invention using a semi-planar architecture.

[0014]   Fig. 4 shows a cross-sectional view of a VCSEL in accordance with an embodiment of the invention using a fully planar architecture.

[0015]   Use of the same reference symbols in different figures indicates similar or identical items.

DETAILED DESCRIPTION

[0016]   In accordance with an aspect of the invention, an optoelectronic device such as a vertical cavity surface emitting laser (VCSEL) includes a tunnel junction that is made inoperative in selected regions to confine current to a desired region, e.g., to where the tunnel junction is operable.

[0017]   Fig. 1 schematically shows a cross-section of a VCSEL 100 in accordance with an embodiment of the invention. VCSEL 100 includes a bottom reflector 110, an active layer 120, a p-type semiconductor layer 125, an n-type semiconductor layer 140, an index guide 160, and a top reflector 170.

[0018]   Bottom reflector 110 is a highly reflective layer such as a distributed Bragg reflector (DBR) that can be formed on an underlying substrate 180. Generally, bottom reflector 110 has a reflectance that is as high as can reasonably be achieved. In VCSEL 100, which has a bottom contact 190 described further below, bottom reflector 110 and substrate 180 are conductive.

[0019]   Top reflector 170 is vertically separated from bottom reflector 110 by a distance that defines the size of the laser cavity of VCSEL 100. Top reflector 170 can similarly be a DBR but has a reflectance and a transmittance selected according to the light amplification in active layer 120. Top reflector 170 transmits the light beam output from VCSEL 100.

[0020]   Active layer 120 is made of a material such as (Al)GaAs or InGaAs(N)/(Al)GaAs that provides induced light emissions in response to light and recombination of electrons and holes in current passing through active layer 120. Layer 120 is typically about 1,000 to 10,000 Å and can be formed by traditional semiconductor crystal growth techniques such as Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE) on bottom reflector 110. In this embodiment, layers 110, 120 125, 130, 140 and 160 are semiconductor layers grown on substrate 180 in a single growth. In a typical embodiment of VCSEL 100, active layer 120 is undoped.

[0021] Layer 125 is p-doped to help support the relatively large reverse voltages across the disabled section of the tunnel junction, and to help transport holes to the active region with low resistance. The doping and thickness of layer 125 would generally be the minimum required to achieve these goals, in order to avoid optical loss associated with p-type doping and to avoid unnecessary lateral spreading of the holes injected from the operable portion of the tunnel junction. In an alternate embodiment, layer 125 could be integral with the heavily doped p-type half of tunnel junction 130.

[0022] N-type layer 140 similarly contains a semiconductor material such as GaAs typically about 1,000 to 5,000 Å thick but has an n-type doping.

[0023] A tunnel junction 130 is at the interface between layers 125 and 140. Tunnel junction 130 includes a thin heavily doped p++ layer (not shown) next to p-type layer 125 and a thin heavily doped n++ layer (not shown) next to n-type layer 140. In an exemplary embodiment of the invention, the thin p++ layer is about 200 Å or less thick and has a dopant concentration of about 1×10^{19} to 1×10^{20} cm^{-3}. The thin n++ layer is similarly about 200 Å or less thick and has a dopant concentration of about 1 to 5×10^{19} cm^{-3}.

[0024] Tunnel junction 130 can be formed by first depositing active layer 120 and p-type layer 125, changing the growth environment to deposit the thin layer having intrinsic p++ doping, changing the growth environment again to deposit the thin layer having intrinsic n++ doping, and finally depositing n-type layer 140.

[0025] The tunnel junction requires extraordinarily high doping levels, which often requires that the growth conditions for the tunnel junction layers be different from the growth conditions for active region 120 and surrounding layers 125 and 140. Besides adding high fluxes of the dopant species to the growth chamber, other growth conditions may also be changed to enhance the incorporation of the dopants into the semiconductor material. For example, in MOCVD growth, lowering the substrate temperature and reducing the ratio of the flow rate of group V element (typically As or P) carrier gases to the flow rate of the group III (typically In, Ga, or Al) carrier gases can enhance the incorporation of carbon, a p-type dopant, and allow the very high doping levels required for efficient tunneling. In MBE, the growth rate might be lowered to allow a higher ratio of flux of dopant atoms to flux of base material atoms. The specific conditions required to achieve extremely high doping levels will

vary with the particular semiconductor being doped, the growth method used, the type of dopant, and even the particular model or brand of growth chamber.

[0026] In operation, n-type layer 140 is positively biased via a ring-shaped electrode 150 and active layer 120 is negatively biased via electrode structure 190 on the back surface of device 100. The bias voltage, which is typically about 2 volts for a conventional VCSEL, provides a reverse bias for a conventional NP junction. However, tunnel junction 130 conducts a current arising from quantum tunneling of electrons from the p++ layer of tunnel junction 130 to the n++ layer of tunnel junction 130, generating a corresponding electron current in n-type layer 140 and a hole current in active layer 120.

[0027] In accordance with an aspect of the invention, a current blocking region 135 formed in tunnel junction 130 confines the current to a portion of active region 120 under index guide 160. With tunneling disabled, current blocking region 135 operates as an ordinary reversed biased PN junction to prevent current flow outside of the desired area of active layer 120. Accordingly, recombination of electrons and holes from the tunneling current through tunnel junction 130 emits light in the laser cavity.

[0028] Blocking region 135 can be formed by any mechanism that disrupts tunneling through tunnel junction 130. One way to disrupt tunneling is to selectively implant dopants at a dose sufficient to render tunneling inoperative. The implantation can be performed through n-type layer 140 and therefore avoids the need to remove and return a wafer to a deposition chamber between formation of layers 120 and 140. Implantation disrupts tunneling by changing the doping profile of selected areas and/or disrupting the crystal lattice.

[0029] An advantage of this approach over a standard current blocking implanted device is that a small dose can be used because the implant only needs to disrupt tunneling and does not need to make the material non-conductive. In addition, this implant needs only affect the thin tunnel junction region, and therefore may be done with a single-energy implant. This is in contrast to a traditional implant-confined VCSEL, in which the ion implantation must render the semiconductor nonconductive throughout several microns of depth..

[0030] In the exemplary embodiment of the invention, for a tunnel junction located 3000Å beneath the surface, a Beryllium implant of 100 keV with a dose of only about 1×10^{11}

/cm^2 would be sufficient to compensate the dopants on the n-type side of the tunnel junction to a sufficient degree to virtually eliminate tunneling current. The smaller dose causes less damage, resulting in fewer defects that can affect reliability of the device. If a subsequent anneal is used in an impurity-induced disordering process as described below, an even lower implant dose could be used.

[0031] The tunnel junction helps to normalize or distribute the current density so that less current is crowded adjacent to the implant. Since VCSEL reliability is typically exponentially dependent on current density, the reduction in peak current density due to the current normalization can further improve device reliability. Another benefit of the current normalizing effect is a wider range of single-spatial-mode operation for VCSELs. Higher current injection near the edge of the confining aperture often creates a spatially nonuniform gain profile in conventional VCSELs which encourages the operation of multiple higher-order transverse spatial modes. Achieving a spatially uniform gain profile would increase the range of currents for which the fundamental lateral mode dominates the lasing action. This single-mode operation can be a vitally important property for VCSELs in communications applications.

[0032] Disordering can also render tunnel junction 130 inoperative in blocking region 135. Disordering makes the transitions between lightly and heavily doped regions less abrupt and thereby prevents significant tunneling current. If the disordering is impurity based, the addition of impurities, typically introduced via implantation, will accelerate the diffusion between the tunnel junction layers. An anneal process of time and temperature sufficient to cause slight diffusion of the tunnel junction layers where the impurities were implanted, but leave other regions relatively unchanged will normally follow the impurity implantation. Spatially patterning the implant of impurities, such as with a mask, can define apertures of operative tunnel junction.

[0033] Impurity free disordering can be used for ultra-low damage. In an impurity-free disordering process, lattice vacancies rather than impurities are introduced to the semiconductor to accelerate the diffusion process. This is often achieved by placing a silicon oxide cap on the surface of the semiconductor. The cap preferentially absorbs atoms from the semiconductor, leaving lattice vacancies behind. These vacancies diffuse rapidly themselves, and also greatly enhance the diffusion of the semiconductor atoms. If the silicon oxide cap or

other vacancy source is spatially patterned, then an anneal process similar to the one described above could be used to diffuse and therefore destroy the tunneling action of a tunnel junction in a spatially selective way.

[0034] Typical ways of spatially patterning a cap are patterned removal of the cap, forming a patterned blocking layer such as a silicon nitride layer between the cap and the tunnel junction, or varying the distance between the cap and the tunnel junction by etching the semiconductor. Use of a cap to induce vacancies has the advantages of not causing the massive crystal damage associated with ion implantation and of preserving the electrical conductivity of the layers near the surface. These benefits would translate into improved device performance and reliability.

[0035] Yet another technique for disabling tunnel junction 130 in selected areas is to mask and etch all or part of tunnel junction 130 before formation of n-type layer 140. After the patterned etch, a wafer containing the device being manufactured is returned to the deposition chamber for formation of n-type layer 140, which electrodes 150 and index guiding layer 160 contact. With this technique, the current blocking region corresponds to the absence of tunnel junction 130 or of the n++ part of tunnel junction 130. The n-type layer 140 and either the p-type layer 125 or the p++ part of tunnel junction 130 form a reverse biased junction.

[0036] After forming current blocking region 135, device 100 is finished in a conventional manner. In particular, layer 160 is patterned and etched to form an index guide, one or more metal layers are formed and patterned to fabricate bias electrode 150 for n-type layer 140 and a bias electrode 190 for active layer 120. The layers forming top reflector 170 are deposited on index guide 160 and patterned to allow access to the metal contacts.

[0037] A tunnel junction with disabled regions for current confinement can be used in VCSELs having a variety of different architectures. Some of the architectural categories of most interest are those achieving low parasitic resistance and capacitance for high bandwidth operation. Reducing crosstalk between devices is also important, especially for high-bandwidth parallel arrays of devices. While the introduction of the tunnel junction to the structure allows the replacement of low-conductivity p-type material with high-conductivity n-type material for reduced parasitic resistance, oppositely biased layers can have a strong

capacitive coupling through current blocking region 135.

[0038]   Fig. 2 illustrates an embodiment of the invention where a VCSEL 200 has a conductive n-type layer 220 underlying active layer 120, while a lower mirror 210 and a substrate 280 are nonconductive. In this embodiment, a lower contact 290 to the device is made from the top by etching that exposes n-type layer 220. The etching for the lower contact limits the area in which layers 140 and 120 are in close proximity, causing a corresponding decrease in the capacitance. An isolation trench 230 is then etched through the lower conductive layer 220 to eliminate any conductive path between devices and therefore virtually eliminates electrical crosstalk.

[0039]   Planar architectures are often of interest in the manufacturing of VCSELs because planar or nearly planar surfaces are easier to pattern and coat than surfaces with deep trenches or tall pillars. Fig. 3 shows a VCSEL 300 having a semi-planar architecture in accordance with an embodiment of the invention. Similar to VCSEL 200, VCSEL 300 has a bias electrode 290 for active region 120 on a top surface of VCSEL 300 and in contact with conductive layer 220. Another feature of VCSEL 300 is a full isolation implant 330, which underlies a portion of n-type layer 140 and electrode 150. This isolation implant replaces the isolation trench 230 in VCSEL 200 and renders nonconductive layers 125, 120, and 220 down to nonconductive mirror 210. In addition to providing device isolation in a planar fashion, VCSEL 300 allows isolation implant 330 to extend underneath n-type layer 140 and contact 150 and further reduces parasitic capacitance beyond the reductions that VCSEL 200 achieves.

[0040]   Fig. 4 shows a VCSEL 400 having a fully planar architecture. This embodiment is similar to VCSEL 300 except that an implantation or diffusion process through blocking region 135 and layers 125 and 120 forms the electrical connection to layer 220. An n-type implant or a long contact alloy forming an n-type region 420 between metal bias electrode 490 and n-type layer 220 could implement this. Bias electrode 490 on n-type region 420 thus electrically connects to active layer 120 via region 420 and layer 220. In this implementation, only the top n-type layer 140 needs be etched to isolate region 420 from layer 140, leaving only an extremely shallow step on the wafer surface.

[0041]   Aspects of the invention described above can be used in a number of

optoelectronic devices but are especially suited to VCSELs. For VCSELs, the tunnel junction allows a reduction in the amount of p-type material required in the laser cavity. P-type material generally has lower conductivity and much higher optical losses than does n-type material. Accordingly, exchanging p-type material for n-type material can lower the operating voltage and the resistance of the device while also reducing the required threshold gain. Lower threshold gain results in higher differential gain, which improves the speed and reliability of the devices.

[0042] Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as defined by the following claims.